PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2005/008373	11.03.2005	24.03.2004

International Patent Classification (IPC) or both national classification and IPC
G06F12/08

Applicant
QUALCOMM INCORPORATED

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☒ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this international Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:

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Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ in written format

   ☐ in computer readable form

   c. time of filing/furnishing:

   ☐ contained in the international application as filed.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. II Priority

1. ☒ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has:

   ☒ paid additional fees.

   ☐ paid additional fees under protest.

   ☐ not paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

   ☐ complied with

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☒ all parts.

   ☐ the parts relating to claims Nos.

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-18
	No:	Claims	19-34
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-34
Industrial applicability (IA)	Yes:	Claims	1-34
	No:	Claims	

2. Citations and explanations

   see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item IV

Lack of unity of invention

1 Reference is made to the following document:

D1: HASHIMOTO T ET AL: "A 90 MW MPEG-4 VIDEO CODEC LSI WITH THE CAPABILITY FOR CORE PROFILE" IEICE TRANSACTIONS ON ELECTRONICS, INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG. TOKYO, JP, vol. E86-C, no. 7, July 2003 (2003-07), pages 1374-1384, XP001172046 ISSN: 0916-8524

D2: US-B1-6 272 597 (FU JOHN WAI CHEONG ET AL) 7 August 2001 (2001-08-07)

D3: EP-A- 215 581 (TEXAS INSTRUMENTS INCORPORATED; TEXAS INSTRUMENTS FRANCE) 19 June 2002 (2002-06-19)

2 The International Searching Authority found 2 inventions in this international application as follows:

I. Claims 1-18 directed to:

An integrated circuit comprising:

-a processor core operable to perform data processing for the integrated circuit;

-a cache memory operable to store data for the processor core; and

-an on-chip memory operable to store data for the cache memory,

-wherein the cache memory is filled with data from the on-chip memory for cache misses, and

-wherein the on-chip memory is filled with data from an external memory under user control.

II. Claims 19-34

An integrated circuit comprising a cache controller operable to handle memory transactions for a cache memory and a second memory at two different levels of a cached memory system,

the cache controller including:

-a first address check unit coupled to a first processing unit and operable to determine whether a first memory address for a first memory access by the first processing unit is currently in the cache memory,

-a second address check unit coupled to a second processing unit and operable to determine whether a second memory address fort a second memory access by the second processing unit is currently in the cache memory, and

-a logic unit coupled to the first and second address check units and operable to handle memory transactions for the first and second memory accesses by the first and second processing units.

2.1 They are not so linked as to form a single general inventive concept (Rule 13.1 PCT) for the following reasons:

2.1.1 The prior art represented by document D1 discloses:

An integrated circuit (Fig. 1) comprising:

-a processor core operable to perform data processing for the integrated circuit(Fig. 1 - "VCE (Video Codec Engines)");

-a cache memory operable to store data for the processor core (Fig. 1 - "LM"); and

-an on-chip memory operable to store data for the cache memory (Fig. 1 - "DRAM (16Mb)"),

-wherein the cache memory is filled with data from the on-chip memory for cache misses (page 1375, right column, lines 10-12).

2.1.2 The difference between the subject-matter of the first group of claims and D1 appears to be:

-the on-chip memory is filled with data from an external memory under user control.

This difference has, therefore, to be considered as the special technical feature which defines the contribution of the first group of claims vis-à-vis the prior art D1.

2.1.3 The second group of claims does not comprise the above mentioned special technical feature.

In fact the second group of claims relate to a cache controller in an integrated circuit, the cache controller arbitrating the access of two processing units to two cache memories.

Hence, the first and second group of claims, which do not share the above mentioned special technical feature, cannot be linked by a single inventive concept and consequently a lack of unity has been acknowledged.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

3 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 does not involve an inventive step in the sense of Article 33(3) PCT, for the following reasons:

3.1 D1 discloses:

An integrated circuit (Fig. 1) comprising:

-a processor core operable to perform data processing for the integrated circuit(Fig. 1 - "VCE (Video Codec Engines)");

-a cache memory operable to store data for the processor core (Fig. 1 - "LM"); and

-an on-chip memory operable to store data for the cache memory (Fig. 1 - "DRAM (16Mb)"),

-wherein the cache memory is filled with data from the on-chip memory for cache misses (page 1375, right column, lines 10-12).

3.2 The subject-matter of independent claim 1 differs from the disclosure of D1 in that:

-the on-chip memory is filled with data from an external memory under user control.

3.3 However, filling an on-chip memory with data from an external memory under user control is a common measure in the art.

4 The same reasoning applies, mutatis mutandis, to the subject-matter of the corresponding independent claim 12, which therefore is also considered not inventive.

5 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 14 is not inventive an inventive step in the sense of Article 33(3) PCT, for the following reasons:

5.1 The subject-matter of claim 14 is technically comparable with the subject-matter of claim 1 which has not been considered inventive, see above paragraphs 3-3.3, with the addition of an additional processor operable to perform general-purpose processing and a memory bus coupling the processors to the external memory.

5.2 However, D1 also discloses:

- another processor operable to perform general-purpose processing (Fig.1 -"Programmable DSP"); and

- a memory bus coupling the processors to the external memory(Fig. 1 - "HIF (HOST I/F)").

6 Dependent claims 2-11, 13, 15-18 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of inventive step, see document D1 and the corresponding passages cited in the search report.

7 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 19 is not new in the sense of Article 33(2) PCT, for the following reasons:

7.1 D2 discloses:

An integrated circuit (abstract, "on-chip cache memory") comprising a cache controller (Fig. 1 - blocks 240, 250, 260, 310, 320 can be considered as parts of a single memory controller since they are build in the same chip) operable to handle memory transactions for a cache memory (Fig. 1 -"L0 110") and a second memory(Fig. 1 - "L1 120") at two different levels of a cached memory system, the cache controller including:

- a first address check unit (Fig. 1 - "PHYSICAL ADDRESS 240"; column 3, lines 56-61 -

"physical address comparator **240**") coupled to a first processing unit (Fig. 2 - "420A"; column 7, lines 52-57) and operable to determine whether a first memory address for a first memory access by the first processing unit is currently in the cache memory (column 3, lines 56-61),

- a second address check unit (Fig. 1 - "PHYSICAL ADDRESS 310"; column 4, lines 27-30 - "physical address comparator **310**") coupled to a second processing unit (Fig. 2 - "420B"; column 7, lines 52-57) and operable to determine whether a second memory address for a second memory access by the second processing unit is currently in the cache memory (column 4, lines 27-30), and

- a logic unit coupled to the first and second address check units and operable to handle memory transactions for the first and second memory accesses by the first and second processing units (Fig. 1 - "MUX 260"; column 4, lines 6-9).

7.2 For the sake of completeness, the applicant attention is drawn to the fact, that as an alternative, the features of claim 19 are also disclosed in D2 when cache L1 of figure 1 is considered as the cache memory, the off-chip memory 510 from figure 2 (see, column 7, lines 41-43) as the second memory, the blocks 180, 170, 210, 260, 330, 340 from figure 1 as the blocks of the cache controller, wherein the "BIG TLB 180" and the "L1 CACHE LOOKUP STAGE 330" correspond to the first and second address check unit (column 4, lines 46-66), and the "DATA STAGE MANIPULATION 340" and "MUX 260" of figure 1 correspond to the logic unit (column 4, line 67- column 5, line 10).

8 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 28 is not new in the sense of Article 33(2) PCT, for the following reasons:

8.1 The subject-matter of claim 28 refers to a method technically similar with the subject-matter of claim 19 which has not been considered new, see above paragraphs 7-7.2, with the addition of allowing the first and second processing units to concurrently access the cache memory and the second memory, respectively, if the first processing unit encounters a hit and the second processing units encounters a miss (column 5, line 14- column 6, line 10).

9 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 32 is not new in the sense of Article 33(2) PCT, for the following reasons:

9.1 The subject-matter of claim 32 corresponds in terms of apparatus features with the subject-matter of claim 28 which has not been considered new, see above paragraphs 8-8.1.

10 Dependent claims 20-27, 29-31 and 33-34 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty or inventive step, see documents D2 and D3 and the corresponding passages cited in the search report.

Re Item VIII

Certain observations on the international application

The relative terms **"Direct memory exchange controller"** and **"DME controller"** used in claims 3, 4, 7, 16-18 have no well-recognised meaning and leave the reader in doubt as to the meaning of the technical feature to which they refer, thereby rendering the definition of the subject-matter of said claims unclear, Article 6 PCT.